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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known			
		Application Number	09/802,120		
		Filing Date	March 8, 2001		
		First Named Inventor	Saulsbury, Ashley		
		Group Art Unit	2183		
Sheet	3	of		Examiner Name	
				Attorney Docket Number	016747-012110US

U.S. PATENT DOCUMENTS						
Examiner Initials *	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	AA					
	AB					

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
	AC							
	AD							

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
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AS	A	NUMOMURA Y ET AL: "M32R/D-INTEGRATING DRAM AND MICROPROCESSOR" IEEE MICRO, IEEE INC. NEW YORK, US, vol. 17 no. 6, 1 November 1997 (1997-11-01), pages 40-48, XP000726003; ISSN: 0272-1732.	
AS	B	KOZYRAKIS C E ET AL: "SCALABLE PROCESSORS IN THE BILLION-TRANSISTOR ERA: IRAM" COMPUTER, IEEE COMPUTER SOCIETY, LONG BEACH, CA, US, US vol. 20, no. 0 1 September 1997 (1997-09-01), pages 75-78, XP000730003; ISSN: 0018-9162.	
AS	C	HERRMANN KLAUS, HILGENSTOCK JOERG, PIRSCH PETER: "ARCHITECTURE OF A MULTIPROCESSOR SYSTEM WITH EMBEDDED DRAM FOR LARGE AREA INTEGRATION" 8 October 1997 (1997-10-08), IEEE INTERNATIONAL CONFERENCE ON INNOVATIVE SYSTEMS IN SILICON, PISCATAWAY, NJ, USA; XP002179990	

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Examiner Signature	<i>[Signature]</i>	Date Considered	4/5/04
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Sheet 3 of 3

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<i>AS</i>	AA					
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	AC					
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	AG							
	AH							

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<i>AS</i>	AI	AIMOTO, YOSHIHARU et al.; "A.768G/PS 3.84GB/s 1 W Parallel Image-Processing RAM Integrating a 16 Mb DRAM and 128 Processors"; ISSCC96/Session 23 / DRAM / Paper SP23.3; 1996 IEEE International Solid-State Circuits Conference; pp. 372-373 and 476	
	AJ	BURSKY, DAVE; "Combo RISC CPU and DRAM Solves Data Bandwidth Issues"; Electronic Design; March 4, 1996; pp. 67-71.	
	AK	SAULSBURY, ASHLEY, et al.; "Missing the Memory Wall: The Case for Processor/Memory Integration"; ACM; 1996; pp. 90-101	
	AL	SHIMIZU, TORO, et al.; "A Multimedia 32b RISC Microprocessor with 16 Mb DRAM"; ISSCC96/Session 13 / Microprocessors/Paper FP 13.4; 1996 IEEE International Solid State Circuits Conference; pp. 216-217 and 448	
<i>AS</i>	AM	MITSUBISHI ELECTRIC CORP; Product Specification for Single-Chip 32-Bit CMOS Microcomputer; © May 1998	

Examiner
Signature

Henry Fan

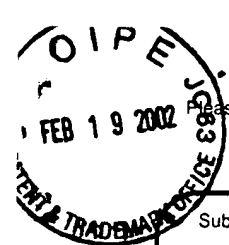
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		Number	Kind Code ² (if known)			
<i>AS</i>	A	4,980,819		Cushing et al.	12/25/1990	RECEIVED FEB 27 2002 Technology Center 2100
<i>1</i>	B	5,530,817		Masubuchi	06/25/1996	
<i>AS</i>	C	5,301,340		Cook	04/05/1994	

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<i>AS</i>	D	PCT	WO 00/33178		Sun Microsystems, Inc.	06/08/2000		

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
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Examiner Name	Unassigned
Attorney Docket Number	016747-012110US

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	AA	US-5,710,907	1/1998	Hagersten et al.	
	AB	US-5,953,738	9/1999	Rao	
	AC	US-6,000,007	12/1999	Leung et al.	
	AD	US-6,128,700	10/2000	Hsu et al.	
	AE	US-6,202,143	3/2001	Rim	
	AF	US-6,256,256	7/2001	Rao	
	AG	US-6,275,900	8/2001	Liberty	
	AH	US-6,321,318	11/2001	Baltz et al.	
	AI				

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		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
	AJ							<input type="checkbox"/>
	AK							<input type="checkbox"/>

NON PATENT LITERATURE DOCUMENTS

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